Discussion of Cold Electronics Development for DUNE/SBND

AUGUST 20TH, 2015

Outline

- Continued Support for Cold Electronics Development
- Accelerated Cold Electronics Development
- SBND Cost Estimate
- DUNE Cost Estimate
- Summary

- Continued (expanded) support for cold electronics development, together with TPC integration, is crucial
 - Cold electronics development (both ASIC design and evaluation test) requires continued support to make steady advancement for various neutrino experiments with final goal to instrument DUNE 10kt
 - To ensure the EE (electrical engineer) readily available when design revision is required
 - Stop-and-go development (supporting development only periodically) is not efficient in a project of this magnitude and in advanced technology
 - MicroBooNE would not be instrumented with FE ASICs without strong support of LBNE LArTPC program
 - Continued support is important for the long term goal of DUNE 10kton installation by ~2020, including various intermediate steps
 - SBND
 - protoDUNE at CERN
 - Vertical slice & production test stands
 - What is shown next is the *minimum* resources required to maintain the cold electronics development efforts

- 1.5 FTE EE/ET per year for cold electronics development in Instrumentation is a reasonable estimate
 - 0.5 FTE EE for ASIC development
 - For limited modifications (FE ASIC with built in pulser, ADC ASIC with improved DNL)
 - 1 FTE EE/ET for cold electronics boards and ASIC test boards development
 - EE should have deep understanding of ASIC evaluation test, such as J. Fried
 - This is a great leverage of Instrumentation resources that BNL has invested in the cold electronics development since 2008
 - ~\$350k labor per year

- Additional (minimum) effort will be required for system integration test and QA/QC in Physics
 - 2.5 FTE EE/PD are required for DUNE and SBND cold electronics development
 - 0.5 FTE EE + 1 FTE EE PD will focus on system integration
 - 1 FTE PD will focus on the evaluation test
 - \$280k ~ \$400k labor per year
 - 1 PD may be covered by base program
 - More scientific effort (BNL, FNAL and collaboration institutes, without project support)

- M&S for prototype submission of two ASICs
 - Fully burdened cost is ~120k with 19% overhead for each submission
 - \$60k for FE ASIC submission will yield 40 chips, additional 40 chips can be obtained at a cost of \$2k
 - Similarly, \$60k for ADC ASIC submission will yield 40 chips, additional 40 chips can be obtained at a cost of \$2k
 - ~\$240k for two prototype submissions for each ASIC to implement and verify design advancements

Accelerated Cold Electronics Development

- It has been discussed recently to accelerate the cold ASICs development, to meet the requirements of both SBND and protoDUNE at CERN
 - Plan to submit the first prototype of FE and ADC ASICs in January 2016
 - Second submission is planned in July/August 2016 after the full evaluation of the first submission
 - Prototype ASICs will be compatible with both FPGA and COLDATA, based on the discussion in July
 - New features will be considered, with careful examination of schedule impact
 - Finalize the list of modifications by early November

Accelerated Cold Electronics Development

- To accelerate the cold ASICs development, more efforts will be needed
 - Two EE graduate students for ASIC design will start in August/ September for two years
 - 0.5 FTE EE for ASIC development to account for increased scope of ASIC revision and supervision of students
 - \$50k each student per year, \$100k per year
 - License of ASIC development tools, \$100k per year
 - One license seat shared by two students
 - Students will contribute to ASIC design, simulation, documentation, evaluation test and get it ready for production submission for SBND and protoDUNE in 2017
 - In summary: ~\$200k in addition per year to accelerate the ASIC developments, or ~\$400k for two submissions in two years

SBND Cost Estimate

- SBND budget covers one prototype submission for each ASIC
 - 1. 0.5 FTE ASIC design EE for revision of two ASICs for limited scope of modifications
 - 2. ~\$120k for one prototype submission for each ASIC
 - 3. 1.5 FTE EE/ET for cold electronics boards and ASIC test boards development, system integration test and QA/QC
- The SBND fund arrived at BNL only covers item 3) cold electronics boards and ASIC test boards development
 - It is ~\$350k
 - It may be re-purposed to cover item 1) and 2) the ASIC development and submission if approved

DUNE Cost Estimate

- There is ~\$150k planned for FY16 cold electronics development in the current schedule
- There is ~\$640k planned for FY16 protoDUNE cold electronics production
- If protoDUNE production fund can be re-purposed, there will be ~\$790k available for cold electronics development in FY16
 - Can not all be re-directed, as it will impact other developments (cold cable, feed-through etc.)

FE/ADC Chip Production Plan in FY17

- SBND and protoDUNE will need ~2,000 FE ASICs and ~2,000 ADC ASICs
 - 704 for SBND + 960 for protoDUNE + 20% spares
- Two options (no overhead is included)
 - Option 1: MPW run with additional wafers
 - \$150k for FE ASIC and \$150k for ADC ASIC, total \$300k
 - ~\$50k for MPW run, 50 additional wafers (40 chips per wafer) @ ~\$2k each
 - Option 2: Dedicated run with additional wafers
 - ~\$250k for both FE and ADC ASICs
 - One mask for both FE and ADC ASICs
 - ~\$200k for mask of dedicated run, 25 additional wafers (180 FE + 180 ADC chips per wafer) @ \$2k each
 - Will get ~5,000 chips for each ASIC

Cost Estimate

- We will need to verify if combined SBND/DUNE budget can cover
 - Two prototype submissions of each ASIC
 - Both labor and M&S
 - Cold electronics boards development, system integration test and QA/QC of SBND and protoDUNE at CERN
 - Both labor and M&S
 - Additional efforts to accelerate the development
 - ~\$200k per year for 2 years
- More details of the cost estimate will be provided in the next slides

Summary of Cost Estimate

FY16 (not including collaboration support of QA)

FY16	Existing Schedule		Accelerated Schedule	
1110	Effort	Cost	Effort	Cost
ASIC Development	0.5 EE		0.5 EE + 2 GS	
Board Development	1 EE		1 EE	
Labor		\$ 350,000		\$ 450,000
System Integration	2.5 EE/PD		2.5 EE/PD	
Labor		\$ 280,000		\$ 280,000
ASIC Submission				
M&S		\$ 120,000		\$ 240,000
CAD Tool				
M&S		\$ -		\$ 100,000
Total		\$ 750,000		\$1,070,000

FY16 Fund Summary		
SBND Fund @ BNL	\$	350,000
SBND ASIC Dev Fund	\$	250,000
DUNE Cold Elec Fund		150,000
protoDUNE Production Fund	\$	640,000
Total		,390,000

- Can we re-purpose the SBND fund arrived at BNL?
- Can we re-purpose the DUNE fund?
 - The impact on other developments (cold cable, feed-through etc.) will have to be examined

Summary of Cost Estimate

• FY17(not including collaboration support of QA)

FY17	Existing Schedule		Accelerate Schedule	
1117	Effort	Cost	Effort	Cost
ASIC Development	0.5 EE		0.5 EE + 2 GS	
Board Development	1 EE		1 EE	
Labor		\$ 350,000		\$ 450,000
System Integration	2.5 EE/PD		2.5 EE/PD	
Labor		\$ 280,000		\$ 280,000
ASIC Submission				
M&S		\$ 120,000		\$ -
CAD Tool				
M&S		\$ -		\$ 100,000
ASIC Production				
M&S		\$ 300,000		\$ 300,000
Total		\$1,050,000		\$1,130,000

FY17 Fund Summary		
SBND Fund	\$	350,000
SBND ASIC Dev Fund	\$	=
DUNE Cold Elec Fund		250,000
protoDUNE Production Fund	\$	280,000
		·
Total	\$	880,000

 DUNE cost and schedule will have to be examined for protoDUNE production and other developments for FY17 & beyond